1-13 (Canceled).

14. (Currently Amended) A silicon over insulator (SOI) metal oxide silicon field effect transistor (MOSFET) device comprising:

a body that is floating with respect to an underlying substrate;

a gate opposite said body;

an RC discriminator comprising a resistor and a capacitor, wherein said RC discriminator is connected to said gate at a point of said RC discriminator between said resistor and said capacitor; and

a circuit control network connected to said body, said circuit control network modulating a potential voltage of said body to provide electrostatic discharge (ESD) protection.

15. (Withdrawn) The device in claim 14, wherein said circuit control network is connected to said gate.

16. (Canceled).

17. (Previously Presented) The device in claim 14, wherein said circuit control network limits said body to a reference voltage.

18. (Previously Presented) The device in claim 14, wherein said circuit control network comprises at least one SOI MOSFET.

19. (Withdrawn) The device in claim 14, wherein said circuit control network comprises at least one ESD SOI diode.

20. (Withdrawn) The device in claim 14, wherein said circuit control network comprises at least one body/gate-coupled SOI diode.

21. (Canceled).

22. (Withdrawn) The device in claim 14, further comprising:

an input pad connected to said gate;

a drain adjacent said gate; and

a source opposite said drain,

wherein said circuit control network is connected to said input pad and said drain and said source is connected to Vss.

23. (Canceled).

24. (Currently Amended) A silicon over insulator (SOI) metal oxide silicon field effect transistor (MOSFET) device comprising:

an n-channel SOI MOSFET comprising a first body that is floating with respect to an underlying substrate and a first gate opposite said first body;

a p-channel SOI MOSFET connected to said n-channel SOI MOSFET, wherein said p-channel SOI MOSFET comprises a second body that is floating with respect to said underlying substrate and a second gate opposite said second body;

a first RC discriminator comprising a first resistor and a first capacitor, wherein said first RC discriminator is connected to said first gate at a point of said first RC discriminator between said resistor and said capacitor;

a second RC discriminator comprising a second resistor and a second capacitor, wherein said second RC discriminator is connected to said second gate at a point of said second RC discriminator between said resistor and said capacitor;

a first circuit control network connected to said first body, said first circuit control network modulating a potential voltage of said first body to provide electrostatic discharge (ESD) protection; and

a second circuit control network connected to said second body, said second circuit control network modulating a potential voltage of said second body to provide electrostatic discharge (ESD) protection.

25. (Previously Presented) The device in claim 24, wherein said first circuit control network and said second circuit control network comprise at least one SOI MOSFET.

26. (Previously Presented) The device in claim 24, wherein said n-channel SOI MOSFET further comprises a first source and a first drain, wherein one of said first source and said first drain is connected to said first resistor and the other of said first source and said first drain is connected to said first capacitor; and

wherein said p-channel SOI MOSFET further comprises a second source and a second drain, wherein one of said second source and said second drain is connected to said second resistor and the other of said second source and said second drain is connected to said second capacitor.

27. (Previously Presented) The device in claim 24, wherein said first resistor and said first capacitor initiate coupling of said first gate when an overvoltage or overcurrent condition exists; and

wherein said second resistor and said second capacitor initiate coupling of said second gate when said overvoltage or overcurrent condition exists.

28. (Previously Presented) The device in claim 24, wherein said first circuit control network limits said first body to a reference voltage, and said second circuit control network limits said second body to said reference voltage.

29. (Previously Presented) The device in claim 24, wherein said first circuit control network and said second control network are coupled to different reference voltages.

30. (Previously Presented) The device in claim 24, further comprising a pad connected between said n-channel SOI MOSFET and said p-channel SOI MOSFET.

31. (Previously Presented) A silicon over insulator (SOI) metal oxide silicon field effect transistor (MOSFET) device comprising:

a silicon-over-insulator body that is floating with respect to an underlying substrate;

a gate opposite said body;

an RC discriminator comprising a resistive transistor and a capacitor, wherein said RC discriminator is connected to said gate at a point of said RC discriminator between said resistive transistor and said capacitor; and

a circuit control network connected to said body, said circuit control network modulating a potential voltage of said body to provide electrostatic discharge (ESD) protection.

32. (Previously Presented) The device in claim 31, wherein said circuit control network limits said body to a reference voltage.

33. (Previously Presented) The device in claim 31, wherein said circuit control network comprises an SOI MOSFET.

34. (Previously Presented) The device in claim 31, further comprising a source and a drain, wherein one of said source and said drain is connected to said resistive transistor and the other of said source and said drain is connected to said capacitor.

35. (Previously Presented) The device in claim 31, wherein said resistive transistor and said capacitor initiate coupling of said gate when an overvoltage or overcurrent condition exists.

36. (Previously Presented) The device in claim 31, further comprising a pad connected to said capacitor.